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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/382,182	08/24/1999	YOSHIO HAGIWARA	12052.20US01	4904

23552 7590 12/21/2001

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EXAMINER
GOUDREAU, GEORGE A

ART UNIT	PAPER NUMBER
1763	9

DATE MAILED: 12/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09-382,182	Applicant(s) Hagiwara
	Examiner George Gaudreau	Group Art Unit 1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 11-01 (Ce - paper # 8)

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-8 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-8 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ Th proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ Th drawing(s) filed on _____ is/are objected to by the Examiner

☐ Th specification is objected to by the Examiner.

☐ Th oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____ .

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____ .

Attachment(s)

☒ Information Disclosure Stat ment(s), PTO-1449, Paper N (s). 6

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Pat nt Drawing Review, PTO-948

☐ Int rview Summary, PTO-413

☐ N tice of Inf rmal Pat nt Application, PTO-152

☐ Other _____

Office Action Summary

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Chen et al. (5,858,869) or Lou (5,759,906).

Chen et. al. disclose a process for forming a via on a wafer which is comprised of the following steps:

-A pad SiO2 layer (12) is formed onto the surface of the Si wafer (10).;

-A PECVD TEOS type SiO2 layer (18) is formed onto the surface of the pad SiO2 layer (12).;

-A patterned Cu wiring layer (16) is formed onto the surface of the PECVD SiO2 layer (18).;

-A PECVD TEOS type SiO2 layer (18) is formed onto the surface of the wafer, and the Cu wiring layer (16).;

-A low K dielectric layer (20) such as polysilsequioxane (i.e.-a Si polymer) is used to planarize the surface of the wafer.;

-An FSG layer (22) is formed onto the low K dielectric layer (20).;

-A patterned photo resist etch mask (24) is formed onto the surface of the FSG layer (22).;

-A via hole is etched through the insulating layers (FSG-low k dielectric-SiO2) which comprise the ILD layers until the surface of the Cu wiring layer (19) is reached.; and

-A conductor is deposited onto the surface of the ILD layer as well as inside the via hole.

This is discussed specifically in columns 1-4; and discussed in general in columns 1-12.

This is shown specifically in figures 3-4; and shown in general in figures 1-13.

Lou discloses a process for forming a via on a wafer which is comprised of the following steps:

-A pad SiO2 layer (12) is formed onto the surface of a Si wafer (10).;

-A patterned wiring layer (16) is formed onto the surface of the pad SiO2 layer (12).;

-A PECVD TEOS type SiO2 layer (18) is conformably formed onto the surface of the wafer.;

-A siloxane type SOG layer (20) is conformably formed onto the surface of the PECVD SiO2 layer (18).;

-A PECVD TEOS type SiO2 layer (22) is conformably formed onto the surface of the SOG layer (20).;

-A via hole (24) is etched through the SiO2 / SOG / SiO2 layers which comprise the ILD.; and

-A conductor (26) is formed onto the surface of the SiO2 layer (22) as well as inside the via hole (24).

This is discussed specifically in columns 4-8; and discussed in general in columns 1-12.

This is shown specifically in figures 3-11; and shown in general in figures 1-11.

These references fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific methods for forming the low K dielectric layer which are claimed by the applicant;

-the specific production of a low K dielectric with the specific dielectric constants, and C contents which are claimed by the applicant; and

-the specific usage of the process taught above for forming the ILD layer in a process for making a damascene

It would have been obvious to one skilled in the art to employ any of the methods for forming an ILD layer in the processes taught above in the formation of an ILD on a wafer in which a damascene type structure is formed based upon the following. This simply represents the usage of an alternative, and at least equivalent means for forming an ILD layer on a wafer in which a damascene type structure is formed to the specific usage of other means for forming such a layer.

It would have been obvious to one skilled in the art to form the SOG layers in any of the processes taught above such that they have the specific dielectric constants, and carbon contents which are claimed by the applicant based upon the following. It would have been desirable to form the SOG layer in the processes taught above such that the SOG layer provides adequate

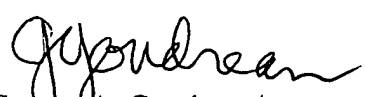
insulation between adjacent circuitry in order to prevent the undesirable cross talk between adjacent layers of circuitry.

It would have been obvious to one skilled in the art to form the SOG layers in any of the processes taught above using the specific methods which are claimed by the applicant based upon the following. The specific methods which are claimed by the applicant for forming the SOG layer are conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming the SOG layer in the processes taught above to the specific usage of other such means.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.



George A. Goudreau/gag

Examiner AU 1763